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# Fabrication and Characterization of Heterojunction for CdS Thin Films and $CuAlO_2$ Ceramic Pill Substrate.

**Thitinai GAEWDANG[1], Ngamnit WONGCHAROEN[1], Adison NOPPARUCHIKUN[1*], Tiparatana WONGCHAROEN[2], and Chaisingh POO-RAKKIAT[3]**

*[1] Department of Physics, Faculty of Science, King Mongkut's Institute of Technology Ladkrabang, 1, Soi Chalongkrung 1, Ladkrabang District, Bangkok 10520, Thailand.*
*[2] Department of Electrical Engineering, School of Engineering, Bangkok University, Klongluang District, Pathumtani, 10220, Thailand.*
*[3] Department of Physics, Faculty of Science, Chulalongkorn University,Phayathai Rd., Pathumwan, Bangkok 13330,Thailand.*

## Abstract

In this research paper, CdS thin films were deposited by thermal evaporation in vacuum on $CuAlO_2$ ceramic pill substrate. From the data of I-V measurements at low temperature (20-300 K) the junction barrier height, ideality factor and series resistance values can be evaluated by using thermionic emission (TE) theory and Cheung's method. The junction barrier height and ideality factor were found to be strong temperature dependence. Evaluation of forward I-V data reveals a decrease in the zero-bias barrier height, but an increase in the ideality factor with decrease in temperature. In part of C-V measurements at room temperature, the obtained built-in potential value being 0.586 V is well consistent with the junction barrier height value evaluated from I-V measurements.

**Key words:** CdS/$CuAlO_2$ heterojunction, I-V measurements, C-V measurements.

## Introduction

CdS thin films are considered at present one of the most promising material for making window layer of CdS/$CuInGaSe_2$ and CdS/CdTe solar cells. $CuAlO_2$ has attracted much attention due to its transparent nature for visible region and p-type conductivity.(2) Transparent p-n heterojunction diode exhibiting a rectifying I-V characteristics was fabricated using a combination of p-$CuAlO_2$/ n-$Zn_{1-x}Al_xO$. Moreover, CdS and $CuAlO_2$ thin films are also interested in optoelectronic devices because it can be prepared in several ways. CdS thin films is well-known to be one of high optical transparency, it is expected that the junction of CdS and $CuAlO_2$ has potential abilities is not only rectifiers but also photovoltaic devices. In this paper, CdS thin films were deposited by thermal evaporation on $CuAlO_2$ ceramic pill substrate. We investigated I-V and C-V characteristics of CdS/ $CuAlO_2$ heterojunction for evaluating some important parameters such as junction barrier height, ideality factor and series resistance values by using thermionic emission theory and Cheung's method.

## Materials and Experimental Procedures

CdS thin films were deposited by thermal evaporation in vacuum better than $3*10^{-5}$ mbar for 40 min on $CuAlO_2$ ceramic pill substrate. $CuAlO_2$ ceramic pill substrate was prepared from mixture of high-purity grade of CuO and $Al_2O_3$ powders. The resulting powders were pressed into pellet form of 1 mm thick and 10 mm diameter and sintered at 1100°C for 48 hours in air. Successful heterojunction device was obtained by annealing in a pure nitrogen atmosphere at 400°C for 30 min. The crystal structure of CdS/$CuAlO_2$ heterojunction device was checked by X-ray diffraction technique with a Brucker D8 diffractrometer using $CuK_\alpha$ radiation ($\lambda$=1.5418Å) at room temperature. Grain size and surface morphology was obtained using Scanning Electron Microscope (SEM). Ohmic contact was made of silver paste on the surface of CdS and on the back surface of $CuAlO_2$. The I-V characteristic curve was measured by using a computer interfaced Keithley 236 current/voltage source at various temperatures. The C-V measurements were carried out by Agilint E4980A Precision LCR Meter with

*Corresponding author E-mail: address: lek-221@hotmail.com

reverse bias from -2.5 to 1.0 V at room temperatures and frequency at 1 MHz.

## Results and Discussion

### *Structural Properties*

XRD patterns of CdS thin films deposited on $CuAlO_2$ pill substrate are shown in Figure 1. Along with the $CuAlO_2$ polycrystalline substrate peaks, a small peak at 27.80° attributed to the diffraction of (002) CdS plane belonging to wurtzite structure was observed. The rest peaks situated at diffraction angle (2θ) higher than 30° is belong to $CuAlO_2$ delafossite structure.

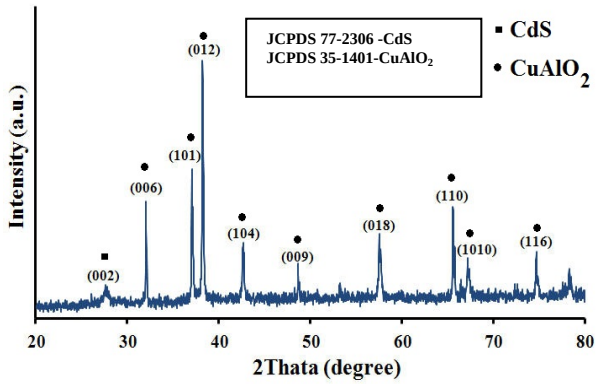
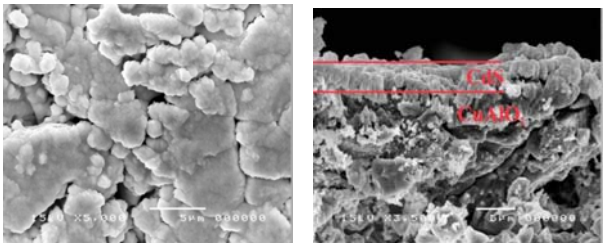



**Figure 1.** XRD patterns of $CdS/CuAlO_2$ heterojunction.

### *Surface Morphological Analysis*

SEM micrographs of $CdS/CuAlO_2$ heterojunction device are shown in Figure 2. $CuAlO_2$ pill substrate exhibits a various grain size while CdS thin films show a very fine grains. From the cross section image (Figure 2b) CdS thin films layer with thickness about 1 μm was also observed.




(a) (b)

**Figure 2**. SEM image of $CdS/CuAlO_2$ heterojunction showing top view image (a) and cross section image (b).

### *I-V Characterization*

In the literature reviews, CdS compound has a higher resistivity than $CuAlO_2$ and carrier concentration of CdS ($<10^{14}$ $cm^{-3}$) is lower than $CuAlO_2$ ($>10^{16}$ $cm^{-3}$) about 3 order. Therefore, in the view of large different carrier concentration between CdS and $CuAlO_2$, it may be assumed that this heterojunction act as nearly a step junction. Therefore, it may assumed that the current through a diode at a forward bias V, based on the thermionic emission (TE) theory, is given by the relation[4]

$$I=I_s\left\{\exp\left(\frac{qV}{nkT}\right)[1-\exp(-qV/kT)]\right\} \quad (1)$$

and $$I_s = A A^* T^2 \exp\left(-q\phi_{B0}/kT\right) \quad (2)$$

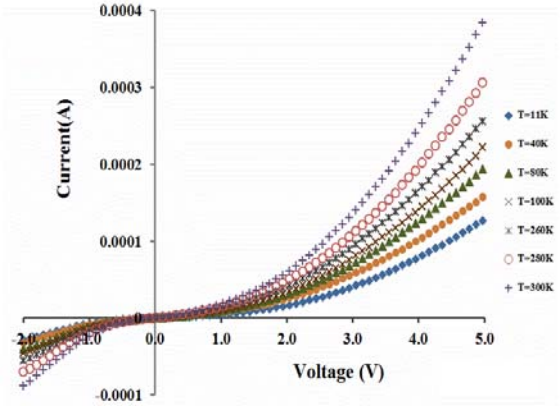



**Figure 3**. The measured I-V plot of $CdS/CuAlO_2$ heterojunction at various temperatures.

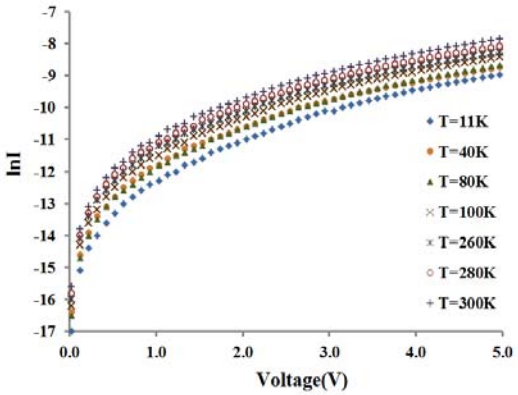



**Figure 4**. The semilogarithmic forward bias I-V plots of $CdS/CuAlO_2$ heterojunction at various temperatures.

where $I_S$ is the saturation current derived from the straight line intercept of the semilogarithmic I-V plot at V=0, V is forward bias voltage, $R_S$ is series resistance, T is the absolute temperature, q is the

electronic charge, k is Boltzmann constant, A is the effective area, $A^* = \frac{4\pi q m_e k^2}{h^3}$ is the effective Richardson constant of 20 A $cm^{-2}K^{-2}$ for n-CdS, where $m^*=0.165m_0$ is the effective mass of the electrons, $\phi_{B0}$ is the apparent barrier height at zere bias voltage and n is the ideality factor. From Eq. (1), the ideality factor n which is given by

$$n=\left(\frac{q}{kT}\right)\left(\frac{dV}{d(\ln I)}\right) \qquad (3)$$

The measured I-V plot of $CdS/CuAlO_2$ diode at different temperatures are shown in Figure 1. We have performed least square fits of Eq. (1) to the linear part of the measured semilogarithmic I-V plots (Figure 3) within bias voltage about 0.2-0.5 V. From these fits, the experimental values of $I_S$ and $\phi_{B0}$ were determined at different temperatures. Once $I_S$ is known, the zero bias barrier height ($\phi_{B0}$) can also be computed with the help of Eq. (2). Using Eqs. (2) and (3), the experimental values of the ideality factor and the barrier height were determined and tabulated in Table 1. The $CdS/CuAlO_2$ diode with a large value of n is far from ideal due to the presence of a thick interfacial layer and the interface states.[4] The non linearlity of I-V characteristics at high bias value indicated a continuum of interface states, which equilibrated with the bulk of semiconductor. The current curve in forward bias quickly becomes dominated by series resistance from contact wires or bulk resistance of the semiconductor, giving rise to the curvature at high current in the semilogarithmic I-V plot. The series resistance $R_S$ is an important parameter in the electrical characteristics of diode. This parameter is significant in the downward curvature (non linear region) of the forward bias I-V characteristics, but the other two parameters ( n and $\phi_{B0}$ ) are significant in both the linear and non linear regions of the I-V characteristics. An efficient technique to determine $R_S$, n and $\phi_{B0}$ has been proposed by Cheung . From Eq. (1) the following functions can be written as

$$\frac{dV}{d(\ln I)}=\frac{nkT}{q}+IR_s \qquad (4)$$

$$H(I)=V-n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \qquad (5)$$

And H(I) is given as follows;

$$H(I)=n\phi_B+IR_s \qquad (6)$$

where $\phi_{B0}$ is the barrier height obtained from data of downward curvature region in the forward bias I-V characteristics. Experimental dV/d(lnI)-I and H(I)-I plots at various temperatures are presented in Figure 5 .Eq. (4) should give a straight line for the data of downward curvature region in the forward bias I-V characteristics. Thus, a plot of dV/d(lnI)-I will give $R_S$ as the slope and nkT/q as the y-axis intercept. Using the n value determined from Eq. (4) and the data of the downward curvature region in the forward bias I-V characteristics in Eq. (5), a plot of H(I)- I will also lead to a straight line with the y-axis intercept equal to $n\phi_{B0}$. The slope of this plot also determines $R_S$, which can used to check the consistency of this approach. Furthermore, the values of $R_S$ obtained from dV/ d(lnI) - I and H(I)- I plots are in good agreement with each other as seen in Table 1. This case shows the consistency of Cheung's approach. As seen from Table 1, the calculated n, $\phi_{B0}$ and $R_S$ were found to be as strongly temperature dependent. Ideality factor greater than 1 has been attributed to particular distribution of interfacial layer and interface states between CdS and $CuAlO_2$. This value of $\phi_{B0}$ calculated from forward bias I-V characteristics have shown an unusual behavior such that it increases with increasing temperature. As can be seen from Figure 6, the value of ideality The high value of the ideality factor show that there is a deviation from TE theory in the current conduction mechanism. The temperature dependence of n suggests that the current conduction mechanism is controlled by the surface states are more pronounced because of the spatial distribution of the interfacial layer of CdS and $CuAlO_2$.

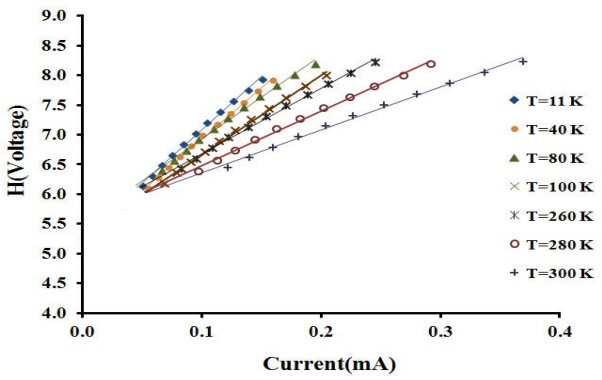



**Figure 5**. H(I)-I plots of $CdS/CuAlO_2$ heterojunction at various temperatures.

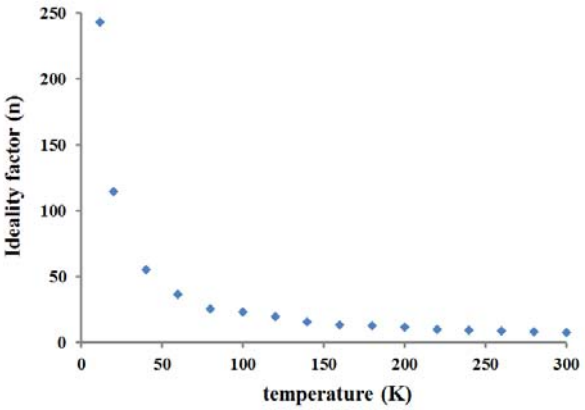



**Figure 6.** The variation of n as a function of temperature of $CdS/CuAlO_2$ heterojunction.

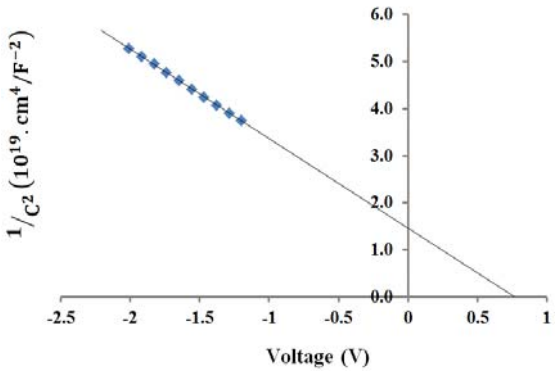



**Figure 7.** $1/C^2$-V plot of $CdS/CuAlO_2$ hetero junction.

**Table 1**. Important parameters determined from I-V characteristics of $CdS/CuAlO_2$ heterojunction at various temperatures.

| Temperature | $I_s$ ($10^{-7}$A) | n | $\Phi_b$ (TE) (eV) | $\Phi_b$ (Cheung's) (eV) | $R_s$ (Ω) |
|---|---|---|---|---|---|
| 20 | 2.45 | 114.432 | 0.032 | 0.032 | 36,770 |
| 40 | 2.78 | 55.237 | 0.068 | 0.067 | 29,808 |
| 60 | 2.83 | 36.830 | 0.106 | 0.106 | 33,473 |
| 80 | 3.60 | 25.830 | 0.144 | 0.141 | 25,061 |
| 100 | 3.78 | 23.410 | 0.183 | 0.186 | 36,811 |
| 120 | 4.04 | 19.817 | 0.222 | 0.224 | 34,308 |
| 140 | 4.41 | 15.832 | 0.262 | 0.265 | 29,808 |
| 160 | 4.64 | 13.752 | 0.302 | 0.309 | 33,473 |
| 180 | 4.82 | 12.785 | 0.343 | 0.348 | 27,566 |
| 200 | 5.24 | 11.810 | 0.386 | 0.389 | 27,976 |
| 220 | 5.54 | 10.012 | 0.469 | 0.432 | 24,818 |
| 240 | 5.71 | 9.758 | 0.514 | 0.472 | 22,210 |
| 260 | 5.82 | 9.012 | 0.559 | 0.513 | 20,793 |
| 280 | 5.97 | 8.291 | 0.606 | 0.553 | 18,952 |
| 300 | 6.08 | 7.895 | 0.593 | 0.596 | 15,296 |

### *C-V Characterization*

The capacitance of the device was measured as a function of applied voltage at a frequency 1 MHz at room temperature. A plot of $1/C^2$ versus applied voltage is shown in Figure7. At the line intercepts on the voltage axis is $V_i$ and we can fine built-in potential ($V_{bi}$) from Eq. 7. The built-in potential value being 0.586 V is well consistent with the junction barrier height value evaluated from I-V measurements. Electron concentration of CdS layer around $4.2\times10^{14}$ $cm^{-3}$ at 300 K evaluated from the slope of $1/C^2$-V plot.[8]

$$V_{bi} = V_i + \frac{kT}{q} \qquad (7)$$

## Conclusion

In summary, *n*-CdS thin films were grown on *p*-$CuAlO_2$ substrate by simple thermal evaporation process. The current–voltage characteristics show rectifying nature, indicating proper formation of the junction. The turn-on voltage is obtained around 0.6 V. The $CdS/CuAlO_2$ heterojunction exhibited a non-ideal behavior with ideality factor of 7.895 at the room temperature. And barrier height was 0.596 V which is similar to built-in potential. The high ideality factor of $CdS/CuAlO_2$ heterojunction is not fully understood, although such high value can be commonly attributed to the interface states and series resistance. So, we will effort to improve the quality of this device.

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